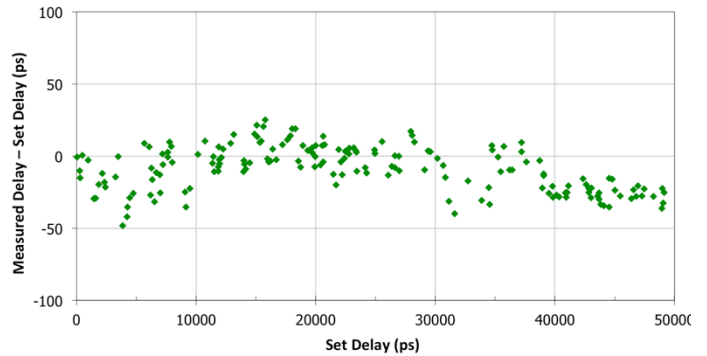
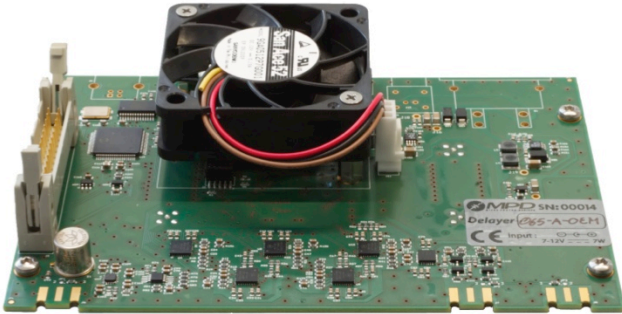




Picosecond Delayer OEM



MPD Picosecond Delayer is a module capable to generate output pulses with user-selectable delay and output pulse duration, in respect to the rising or falling edge of the input signal. This new instrumentation, completely based on solid-state components, sets a new milestone with best in class precision, time-jitter and stability over a wide range of temperatures, not even matched by standard coaxial cables.

- ▶ **Fine adjustable picosecond delayer**
10ps resolution and programmable output width
- ▶ **Very high bandwidth and low jitter**
Up to 380 MHz with random jitter of 5ps RMS
- ▶ **Dual output**
TTL and NIM
- ▶ **High performance uniformity**
INL between +50ps & -100ps
- ▶ **Frequency divider**
Input frequency can be divided by a factor up to 999

MODULE FEATURES

- 50 ns maximum delay range
- 10 ps step
- TTL and NIM output pulses
- up to 380 MHz bandwidth (NIM output)
- programmable output width from 1 ns to 250 ns
- INL between +50 ps and -100 ps over full-scale range and for all temperatures
- random jitter typ. 5 ps RMS
- < 1 ms programming time
- USB interface
- All solid state, no coax cables

BIOMEDICAL APPLICATION

- Correlation Measurements
- Spectroscopy
- Time-correlated single photon counting
- Optical Tomography

INDUSTRIAL APPLICATION

- Streak camera synchronization
- Short gate acquisition experiments

QUANTUM APPLICATION

- Quantum Cryptography
- Single-photon source characterisation

ASTRONOMY APPLICATION

- Optical Range Finding, LIDAR & LADAR

Overview

The MPD Picosecond Delayer is a module capable to generate output pulses (both NIM and TTL) with user-selectable delay and output pulse duration, in respect to the rising or falling edge of an input signal. It can act also as a frequency divider by a user selectable positive integer ranging from 1 to 999. This new instrumentation, completely based on solid-state components, sets a new milestone with best in class precision, time-jitter and stability over a wide range of temperatures, not even matched by normal coaxial cables.

The delayer features a 50 ns nominal full scale range with a 10 ps step delay resolution, whilst the output pulse duration is also user controllable from 1 ns to 250 ns with a nominal step of 3.3 ns.

The excellent integral non linearity error is comprised between +50 ps and -100 ps over the full scale range and for all operating temperatures. This exceptional performance makes the picosecond delayer the perfect choice for any experimental set-up where signals must be delayed with high accuracy and stability of characteristics over a broad range of delays and temperatures.

The low random jitter makes it also successfully suitable in any Time Correlated Single Photon Counting application.

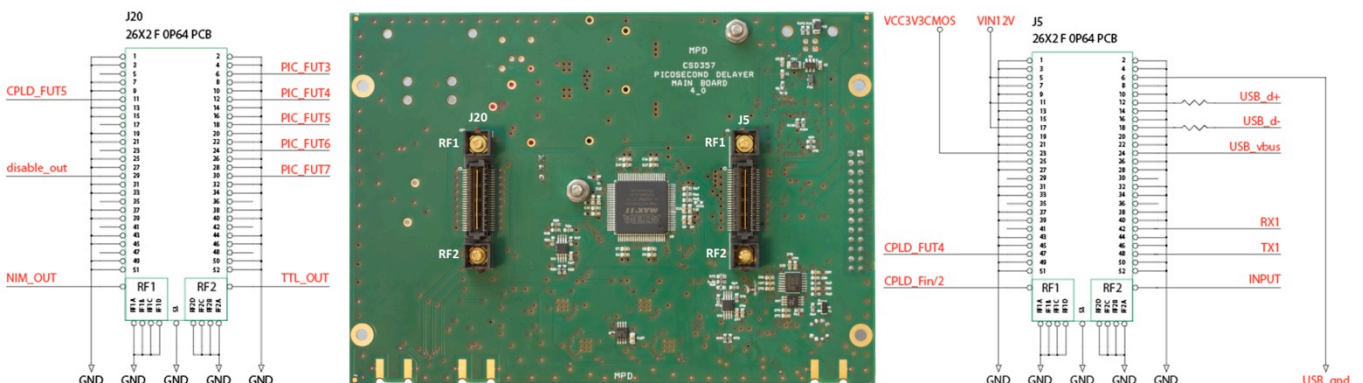
The MPD Picosecond Delayer -OEM version- allows the exploitation of such characteristics, inside custom build instruments, through the use of a compact daughter board.

Board integration

All the signals and power lines are routed and/or fed through two special connectors (J5 and J20), mounted at the bottom of the daughter board and shown here below. Thanks to this connectors it is possible not only to access to the delayer's input and outputs but also to talk directly to the internal microcontroller both via a USB bus (the provided USB driver will create a Serial "Virtual COM" on the host PC, exactly as the one employed in the \$PSD-065-A-MOD) and via an additional UART interface. The communication with the board is obtained by sending ASCII strings over the virtual COM or directly to the Picosecond Delayer microcontroller through the UART interface (pins TX1 and RX1). Other useful signals or still unused lines for future development are also already routed to the special connectors.

The MPD Picosecond Delayer can be operated, for diagnostic purposes, through a PC interface that exploits the USB Virtual Serial COM. Finally, in order to introduce new features or correct found bugs it is possible to update the Picosecond Delayer microcontroller's firmware and the CPLD firmware. This can be achieved through the use of the USB Virtual COM port and a PC with Microsoft Windows® installed. For these reasons, the recommended way of controlling the board is by direct communication through the UART interface, while leaving the USB one only for diagnostic and firmware updates.

The delayer board has been designed with a thermal control loop that, by continuously adjusting the fan rotation speed, sets the board temperature to 55°C with $\pm 0.2^\circ\text{C}$. For this reason, while the board can be successfully inserted in a closed metal box, particular care must be taken on how the complete instrument dissipation is handled or in avoiding thermal gradients on the MPD board. Please contact MPD for further details and support.



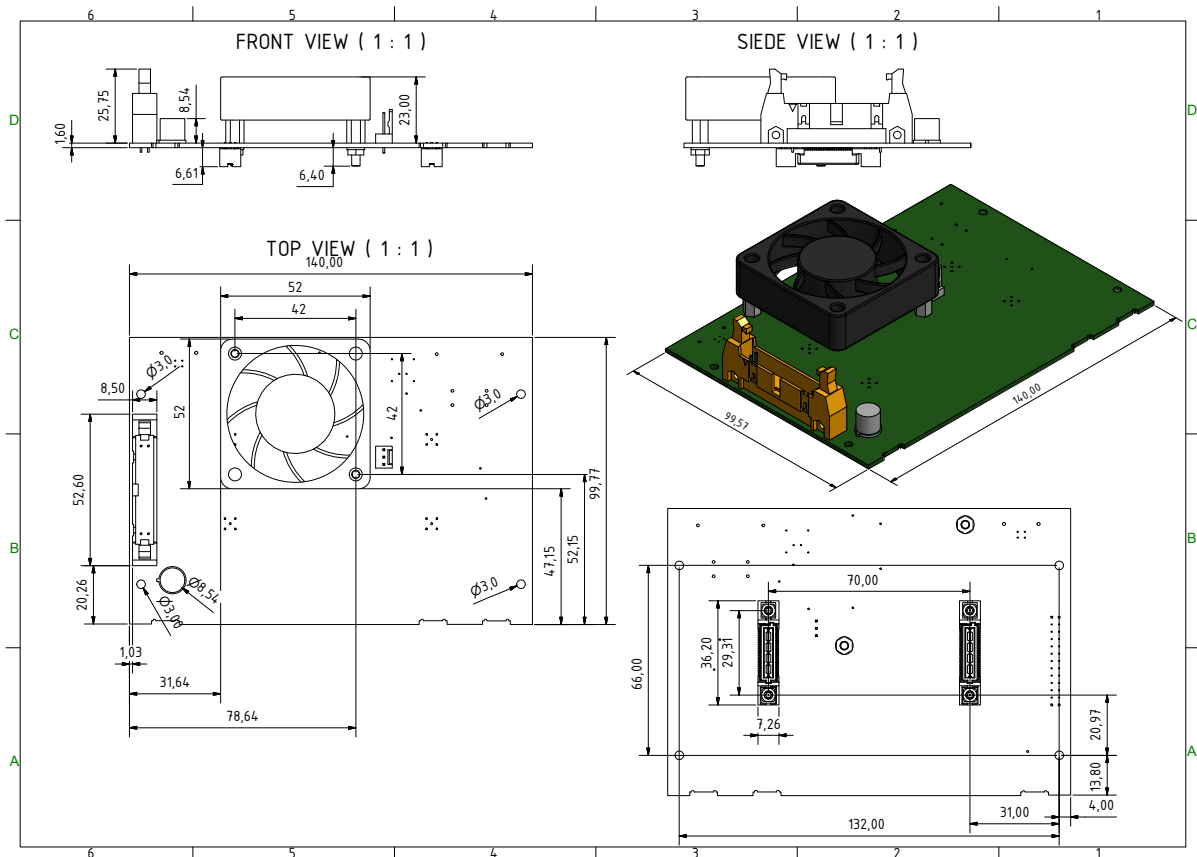
Specifications

| Parameter | Symbol | Description | Min. | Typ. | Max. | Unit |
|---|--|---|------|-------------------------|------|------------------|
| Input high voltage | V_{IN_High} | | | | 3 | V |
| Input low voltage | V_{IN_low} | | -2 | | | V |
| Input differential range | V_{D_MAX} | | -2 | | 2 | V |
| Input termination | R_{IN} | | | 50 | | Ω |
| Input voltage overdrive | V_{OV} | | 100 | | | mV |
| Input pulse width | t_{IN} | | 100 | | | ps |
| Input Slew Rate | SR | | 100 | | | V/ μ s |
| Input overdrive dispersion | | 100 mV < V_{OV} < 1 V | | 10 | | ps |
| Input slew rate dispersion | | 2 V/ns < SR < 10 V/ns | | 15 | | ps |
| Input Edge | | | | Neg/Pos | | |
| Input Threshold | V_{TH} | | -2 | | 2 | V |
| Input threshold resolution | ΔV_{TH} | | 10 | 18 | 30 | mV |
| NIM Output low logic level | V_{NIM_High} | 50 Ω termination required | | 0 | | V |
| NIM Output high logic level | V_{NIM_Low} | 50 Ω termination required | | -800 | | mV |
| NIM Output Bandwidth | BW_{NIM} | | 300 | 380 | | MHz |
| TTL Output Bandwidth | BW_{TTL} | | 100 | 120 | | MHz |
| TTL Output low logic level | V_{TTL_Low} | 50 Ω termination required | | 0 | | V |
| TTL Output high logic level | V_{TTL_High} | 50 Ω termination required | 2.4 | | | V |
| Propagation delay INPUT - NIM OUT | t_{PD_NIM} | | 12 | 15 | 18 | ns |
| Propagation delay INPUT - TTL OUT | t_{PD_TTL} | | 16 | 19 | 22 | ns |
| Delay programmable range | t_{RANGE} | Equivalent to t_{DELAY} (max) | 45 | 50 | 55 | ns |
| Delay programmable range Temperature variation | Δt_{RANGE} (T) | | | 75 | | ps/ $^{\circ}$ C |
| Random timing jitter (RMS) | Rt_{jitter} | $t_{DELAY} = 0$ ns | | 2 | 5 | ps |
| | | $t_{DELAY} = t_{range}$ | | 5 | 12 | ps |
| Delay step | Δt_{DELAY} | | | 10 | | ps |
| Delay integral non linearity | INL | Full scale range | -100 | | 50 | ps |
| Input frequency divider factor | | | 1 | | 999 | |
| OUTPUT pulse duration | t_{OUTPUT} | | 1 | | 250 | ns |
| OUTPUT pulse step | Δt_{OUT} | Pulse width incremental step | | 3.3 | | ns |
| OUTPUT off time | t_{NIM_OFF}, t_{TTL_OFF} | t_{NIM_OFF} and t_{TTL_OFF} are not guaranteed to be the equal. | 1 | 3 | | ns |
| OUTPUT pulse width jitter | t_{OUT_jitter} | % of pulse duration | | | 1 | % |
| OUTPUT pulse width INL | t_{OUT_INL} | Referred to Applied value, NIM OUT | | max ($\pm 5\%$, 1 ns) | | |
| OUTPUT pulse width difference between TTL and NIM (TTL-NIM) | $\Delta t_{TTL-NIM}$ | | | 1 | | ns |
| Programming time | t_{PROG} | Not valid for input edge change | | 1 | 2 | ms |
| 12V Power Supply (INPUT) | VCC12V | 12 V board's power supply | 11 | 12 | 13 | V |
| 3.3V Power Supply (OUTPUT) | VCC3V3CMOS | 3.3V internal logic power supply | 3.2 | 3.3 | 3.4 | V |
| 12V Power supply -current- SINK | VCC12V | Maximum DC current absorbed by the 12V power supply | | | 1 | A |
| 3.3V Power supply -current- SOURCE | VCC3V3CMOS | Maximum current that can be sourced by the 3.3V power supply | | | 500 | mA |
| GND | GND | Board ground | | N/A | | |
| $V_{IL,I/O}$ (I/O INPUT) | RX1, CPLD_FUT_X PIC_FUT_X, Disable_output | | 0 | | 0.4 | V |
| $V_{IH,I/O}$ (I/O INPUT) | RX1, CPLD_FUT_X PIC_FUT_X, Disable_output | | 2.8 | | 3.3 | V |
| $V_{OL,I/O}$ (I/O OUTPUT) | TX1, CPLD_FUT_X PIC_FUT_X, CPLD_Fin/2 | High Z termination | 0 | | 0.4 | V |
| | | 50 Ohm termination | 0 | | 0.2 | V |
| $V_{OH,I/O}$ (I/O OUTPUT) | TX1, CPLD_FUT_X PIC_FUT_X, CPLD_Fin/2 | High Z termination | 2.8 | | 3.3 | V |
| | | 50 Ohm termination | 1.6 | | 2.4 | V |
| CPLD_Fin/2 - frequency | | | 100 | 120 | | MHz |
| USB power supply | USB_vbus | Refer to standard specifications | 4.5 | | 5.5 | V |
| USB data signal plus | UBS_d+ | Refer to standard specifications | | | N/A | |
| USB data signal minus | USB_d- | Refer to standard specifications | | | N/A | |
| USB ground | USB_gnd | Refer to standard specifications | | | N/A | |

System requirements

- USB 1.1 and 2.0 interface
- Picosecond Delayer software
 - Microsoft Windows XP, Vista, 7, 8, 32 or 64 bit versions
- Virtual COM
 - Microsoft Windows XP, Vista, 7, 8, 32 or 64 bit versions
 - Linux Ubuntu 12.04 LTS, Fedora Core 15 or compatible distributions, 32 or 64 bit versions.
 - Mac OS X 10.7.5 and above

Mechanical drawings



Ordering Information

The Picosecond Delayer can be ordered directly from Micro Photon Devices or its representatives. For a complete list of representatives, visit our website at www.micro-photon-devices.com. The ordering code is the following:

\$PSD - 065 - A - OEM

Warranty

A standard legal warranty according to local legislation applies following shipment. Any warranty is null and void if the module case has been opened or if the absolute maximum ratings are exceeded. Specifications are subject to change without any notice. Document version 2.3 – July 2018.

Contacts

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